UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,289	08/21/2003	Son Ho	MP0390.I	9390

26703	7590	07/26/2006	EXAMINER

HARNESS, DICKEY & PIERCE P.L.C.
5445 CORPORATE DRIVE
SUITE 400
TROY, MI 48098

PATEL, KAUSHIKKUMAR M

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/646,289	HO ET AL.
	Examiner	Art Unit	
	Kaushikkumar Patel	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>22 June 2006</u>.

2a)☒ This action is **FINAL**.   2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-17</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-17</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>21 August 2003</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicant's arguments filed June 22, 2006 have been fully considered but they

are not persuasive.

Applicant argues that "Examiner admits that primary reference Zaidi dose not

show, teach or suggest a memory storage system including a line cache that is

accessed by the first CPU". Examiner respectfully disagrees with this. As indicated on

pages 3-4 in previous office action mailed March 23, 2006, Zaidi does teach a first CPU

with cache (with respect to line cache, there is no explicit definition of line cache in the

specification and the broadest reasonable meaning of line cache is that cache divided

into pages, which is well known in the art) (see fig. 1, items 100 and 112). Also

reference made to background of invention regarding an operation of cache (i.e.

processor wanting to access data, first checks in the cache and if data is present in the

cache, data is accessed from the cache and, if data is not present, a miss occurs and

data is loaded from secondary memory into a cache). The intended purpose of

processor having cache is well known in the art, since Zaidi teaches a system, with

multiple processors and caches, inherently teaches processor checking a cache for

presence of data and if data is not in the cache (a miss occurs) and data is brought into

the cache. As stated in previous office action (page 4) Zaidi fails to teach loading of

extra page(s) while loading the page, which caused miss in the cache (i.e. in case of

Zaidi, when miss occurs in the cache, only one page which caused miss is loaded from

lower latency memory. As per applicant's admitted prior art, this is well known in the art, see present application specification, PGPUB par. [0003]). The additional limitation of claim 1, from present application is loading extra pages, with the page, which caused a miss (also known as pre-fetching, pre-loading, look-ached, or demand paging). Loafman teaches benefit of loading extra page(s), with the page that is being loaded from the secondary storage to RAM (RAM is divided in the pages) after a miss (page fault) occurs. Loafman teaches, when data is read sequentially from the secondary storage (higher latency storage), loading as much data as possible into RAM (lower latency storage than secondary storage) improves the performance of the system, as when next page is needed, it is already present in the RAM (due to pre-fetching) and thus avoids another page fault (miss) and latency of loading page from secondary high latency storage. Thus Loafman teaches advantage of pre-fetching multiple pages during sequential access of data (see Loafman par. [0012], Spatial data pre-fetching works splendidly well). Applicant's argument about establishing prima facie case of obviousness is that one having ordinary skill in the art would be motivated to use pre-fetching of data as taught by Loafman in the system of Zaidi to improve system performance by reducing page faults (or cache miss) by pre-loading as much data as possible because there is a high probability of spatial data being accessed next.

2.   The rejection of claims is respectfully maintained as explained above and reiterated below for applicant's convenience.

Priority

3.   The later-filed application must be an application for a patent for an invention, which is also disclosed, in the prior application (the parent or original nonprovisional application or provisional application). The disclosure of the invention in the parent application and in the later-filed application must be sufficient to comply with the requirements of the first paragraph of 35 U.S.C. 112. See *Transco Products, Inc. v. Performance Contracting, Inc.*, 38 F.3d 551, 32 USPQ2d 1077 (Fed. Cir. 1994).

The disclosure of the prior-filed application, Application No.10/626507, fails to provide adequate support or enablement in the manner provided by the first paragraph of 35 U.S.C. 112 for one or more claims of this application.

The parent application #10/626507 fails to provide support for pre-fetching data from higher latency memories when cache miss occurs in line cache, accordingly claims 1-2, 5-7, 10, 13-15 are not entitled to the benefit of prior application.

Claim Rejections - 35 USC § 103

4.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1-3, and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Zaidi et al. (US 6,601,126 B1) (Zaidi herein after) and further in view of Loafman

(US 2005/0021916 A1).

As per claim 1, Zaidi teaches memory storage system that is accessed by a first

central processing unit (CPU) (fig. 1, item 100 and item 112), comprising:

a line cache including a plurality of pages that are accessed by the first CPU (fig.

1, item 126. Also caches are known to store pages accessed by CPU, see background

art section of present application); and

a first memory device that stores data that is loaded into said line cache when

miss occurs (fig.1, item 108 is connected to processor via cache 126 to CPU 112,

column 22, lines 65-67, teaches processor use cache to access data from memory 108

and as per present application's background art section, data are loaded from lower

latency memories to cache when miss occurs);

Zaidi fails to teach loading n pages from sequential locations from memory.

Loafman teaches when miss occurs in memory (cache); system preloads consecutive

pages from lower latency storage (paragraph [0026]) into memory. It would have been

obvious to one having ordinary skill in the art at the time of the invention to modify the

memory storage system of Zaidi by prefetching some extra sequential pages when

page fault (cache miss) occurs and the requested page is being loaded from higher

latency storage to memory (cache), because during sequential access of data it is

highly likely that nearby data will be accessed in near future, and by prefetching

adjacent (extra) pages will avoid cache miss next time CPU references the sequential

data and thus, improving the performance (see Loafman paragraphs [0011]-[0013]).

As per claim 2, Loafman teaches that if program continue sequentially accessing

prefetched pages, than prefetching more pages (four and eight and so on) into cache.

(fig. 2, paragraph [0026]).

As per claim 3, Zaidi teaches a second memory device (fig. 1, item 106); and a

line cache control system that controls data flow between said line cache, the first CPU,

said first memory device and said second device (column 4, lines 27-47);

a first line cache interface that is associated with the first CPU, that receives a

first program read request from the first CPU and that generates a first address from

said first program read request (fig. 1, item 116 provides interface to cache. Page 23,

lines 29-31 teach CPU generating address from program read request);

a first memory interface that communicates with said first memory device; a

second memory interface that communicates with said second memory device (fig. 1,

item 104 teaches memory bus connecting first and second memories to cache); and

a switch that selectively connects said line cache to one of said first and second

memory interfaces (fig. 1, item 142, column 5, lines 60-67 to column 6, lines 1-2 and

column 22, lines 40-45) and caches are known to receive addresses from processors

and comparing those addresses to stored addresses and providing data to processor if

hit occurs and loading pages from lower higher latency memory in case of cache miss

(see background of invention in present application). Loading n pages is taught by

Loafman as per reasoning applied to claim 1 above.

Claims 5 and 6 are rejected under same rationales as applied to claims 1 and 2.

As Loafman teaches that as long as CPU accesses data in sequential manner, than

controller keeps prefetching additional pages (2,4,8 etc. Fig. 2, items 210, 220, 230) and

thus next sequential address is already read ahead in the cache and hence no cache

miss occurs.

As per claim 7, Loafman teaches loading 2 pages, then 4 and then 8,

sequentially (fig. 2, paragraph [0026]), which inherently teaches m^{th} page from n pages

(accessing 1st then 2nd and loading 4, and then 8 pages, in case of two pages n = 2 and

reading 2nd page teaches reading m^{th} (2nd) page of two pages or 3rd in case of 4 pages

preloaded and hence m is greater than one and less than or equal to n and prefetching

4 or 8 pages teaches additional n pages).

Claim 8 is rejected under same rationales as applied to claim 3.

Claim Rejections - 35 USC § 103

6.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

7.   Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Zaidi and Loafman as applied to claims 1-3 and 5-8 above, and further in view of

Barroso et al. (US 6,725,334 B2).

As per claims 4 and 9, Zaidi and Loafman teach a dual processor system with two caches (fig. 2, items 202 and 214, first and second processors, and items 208 and 224, two caches). Zaidi and Loafman inherently teach cache interface with first and second CPUs and both generates read requests and hence first and second address as taught in claim 1. Zaidi teaches system with two caches for two processors and Zaidi fails to teach cache arbitration device which communicates with first and second cache interfaces and resolves cache access conflicts between first and second CPUs. Barroso teaches a second level cache with switch (fig. 1, item 130 and 120), which provides interfaces with first and second CPU and arbitrates between first and second CPU (column 4, lines 10-21).

It would have been obvious to one having ordinary skill in the art at the time of invention to modify the multiple cache with multiple processor system of Zaidi and used one cache with switch as taught by Barroso to reduce the cost and the waste of the cache capacity (column 1, lines 45-65).

Similarly claims 10-17 are rejected under same rationales as applied to claims 1-9 above.

Conclusion

8.   **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Kaushikkumar Patel whose telephone number is 571-

272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone

number for the organization where this application or proceeding is assigned is 571-

273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Kaushikkumar Patel
Examiner
Art Unit 2188

7/24/06

MANO PADMANABHAN
SUPERVISORY PATENT E:

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